

WEST Search History

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DATE: Sunday, February 12, 2006

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<i>DB=PGPB,USPT; PLUR=NO; OP=ADJ</i>			
<input type="checkbox"/>	L67	I32 and I2	3
<input type="checkbox"/>	L66	firmware and 164	103
<input type="checkbox"/>	L65	I2 and L64	1
<input type="checkbox"/>	L64	I24 same (I25 or I26)	601
<input type="checkbox"/>	L63	L62 not L58	19
<input type="checkbox"/>	L62	(L55 or L56) and L61	21
<input type="checkbox"/>	L61	(710/260 710/261 710/262 710/263 710/264 710/265 710/266 710/267 710/268 710/269).ccls.	1821
<input type="checkbox"/>	L60	(712/260).ccls.	0
<input type="checkbox"/>	L59	(712/260 712/261 712/262 712/263 712/264 712/265 712/266 712/267 712/268 712/269).ccls.	0
<input type="checkbox"/>	L58	(L55 or L56) and L57	14
<input type="checkbox"/>	L57	(712/244).ccls.	520
<input type="checkbox"/>	L56	(712/229).ccls.	298
<input type="checkbox"/>	L55	(712/43).ccls.	212
<input type="checkbox"/>	L54	6041402.pn.	1
<input type="checkbox"/>	L53	L49 and (interrupt\$1 or exception\$1 or trap\$1)	12
<input type="checkbox"/>	L52	6081890.pn.	1
<input type="checkbox"/>	L51	6272453.pn.	1
<input type="checkbox"/>	L50	6272453.uref.	4
<input type="checkbox"/>	L49	6081890.uref.	21
<input type="checkbox"/>	L48	legacy with L47	7
<input type="checkbox"/>	L47	native with (interrupt\$1 or exception\$1 or trap\$1)	897
<input type="checkbox"/>	L46	multiplexing interrupts	3
<input type="checkbox"/>	L45	native with legacy with (trap\$3 or exception\$1 or interrupt\$3)	7
<input type="checkbox"/>	L44	5608886.pn.	1
<input type="checkbox"/>	L43	dual architecture exception\$1	2
<input type="checkbox"/>	L42	L41 and (interrupt\$3 or exception\$1 or trap\$4)	5
<i>DB=USPT,PGPB; PLUR=NO; OP=ADJ</i>			
<input type="checkbox"/>	L41	('5598546' '5638525' '5774686' '5781750' '5930490')![pn]	5
<i>DB=PGPB,USPT; PLUR=NO; OP=ADJ</i>			

□	L40	non-native mode	33
□	L39	(ia-32 with interrupt\$3) and (ia-64 with interrupt\$3)	5
□	L38	interrupt\$3 and L37	106
□	L37	ia-32 and ia-64	390
□	L36	merced and ia-32	13
□	L35	native same L34	14
□	L34	x86 with interrupt\$1	212
□	L33	x86 interrupt\$1	26
□	L32	(L29 or L30) same L31	127
□	L31	16 bit\$1 with interrupt\$1	1192
□	L30	32 bit\$1 with interrupt\$1	707
□	L29	64 bit\$1 with interrupt\$1	194
□	L28	interrupt\$1 and L27	24
□	L27	L24 same L26	76
□	L26	64 bit\$1 with microprocessor\$1	930
□	L25	32 bit\$1 with microprocessor\$1	3207
□	L24	16 bit\$1 with microprocessor\$1	3332
□	L23	interrupt\$1 and L22	26
□	L22	L14 and L21	40
□	L21	32 bit\$1 with processor\$1	7021
□	L20	L19 and L14	12
□	L19	64 bit\$1 with processor\$1	2793
□	L18	L17 not L15	9
□	L17	L14 same L16	12
□	L16	32 bit\$1 with processor	6360
□	L15	L9 and L14	3
□	L14	16-bit\$1 with coprocessor\$1	108
□	L13	4349873.pn.	1
□	L12	interrupt\$1 and L7	12
□	L11	interrupt\$1 and L6	110
□	L10	L7 and (L9 or L8)	0
□	L9	32-bit processor\$1	789
□	L8	64-bit processor\$1	350
□	L7	16-bit coprocessor\$1	13
□	L6	64-bit processor	266
□	L5	32-bit processor	592
□	L4	16-bit coprocessor	12

□	L3	hardware interrupt\$1 same L1	12
□	L2	interrupt\$1 same L1	96
□	L1	real mode\$1 same protected mode\$1	547

END OF SEARCH HISTORY